CLAIMS

Claim 1 (Original): A signal processing apparatus, comprising:

a channel pooling signal processor, including:

a plurality of computation units;

a test interface for testing the function of said plurality of computation units;

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and

an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and

a digital signal processor connected to said channel pooling signal processor;

wherein said channel pooling signal processor performs more computationally intensive signal processing operations and said digital signal processor performs less computationally intensive signal processing operations.

Claim 2 (Original): The signal processing apparatus of Claim 1, wherein a computation unit of said plurality of computation units comprises:

a data sequencer for controlling program execution;

a configurable logic unit; and

a dedicated memory.

Claim 3 (Original): The signal processing apparatus of Claim 1, further comprising:

a second channel pooling signal processor for processing multiple data streams of voice and data information.

Claim 4 (Original): The signal processing apparatus of Claim 1, wherein said plurality of computation units are heterogenous computation units.

Claim 5 (Original): The signal processing apparatus of Claim 1, wherein said plurality of computation units are homogeneous computation units.

Claim 6 (Original): A method for signal processing, comprising the steps of:

processing high complexity algorithms in a channel pooling signal processor, said channel pooling signal processor including:

a plurality of computation units;

a test interface for testing the function of said plurality of computation units;

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and

an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and

processing low complexity algorithms in a digital signal processor connected to said channel pooling signal processor.

Claim 7 (Original): The method of Claim 6, further comprising the steps of:

controlling program execution in a computation unit of said plurality of computation units;

configuring a configurable logic unit in said computation unit in accordance with a standard; and

storing program execution instructions in a dedicated memory in said computation unit.

Claim 8 (Original): The method of Claim 6, further comprising the steps of.

processing multiple data streams of voice and data information in a second channel pooling signal processor.

Claim 9 (Previously Presented): A base station transceiver comprising:

an antenna for receiving communication signals; and

a signal processing apparatus having:

a channel pooling signal processor, including:

a plurality of computation units;

a test interface for testing the function of said plurality of computation units;

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and

an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and

a digital signal processor connected to said channel pooling signal processor;

wherein said channel pooling signal processor performs more computationally intensive signal processing operations and said digital signal processor performs less computationally intensive signal processing operations.

Claim 10 (Previously Presented): A method for processing communication signals, comprising the steps of:

receiving communication signals;

processing high complexity algorithms on the received communications signals in a channel pooling signal processor, said channel pooling signal processor including:

a plurality of computation units;

a test interface for testing the function of said plurality of computation units;

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and

an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and

processing low complexity algorithms in a digital signal processor connected to said channel pooling signal processor.

Claim 11 (Newly Added): The signal processing apparatus of Claim 1, wherein the computation units are flexibly configured and connected to perform any one of several different transceiver functions.

Claim 12 (Newly Added): The signal processing apparatus of Claim 1, wherein the computation units are configured to perform one or more of downconversion, dechannelization, demodulation, decoding, equalization, despreading, encoding, modulation, spreading, and diversity processing.

Claim 13 (Newly Added): The signal processing apparatus of Claim 1, wherein the computation units support time-division, code-division, and/or frequency division processing.

Claim 14 (Newly Added): The method of Claim 6, wherein the computation units are flexibly configured and connected to perform any one of several different transceiver functions.

Claim 15 (Newly Added): The method of Claim 6, wherein the computation units are configured to perform one or more of downconversion, dechannelization, demodulation, decoding, equalization, despreading, encoding, modulation, spreading, and diversity processing.

Claim 16 (Newly Added): The method of Claim 6, wherein the computation units support time-division, code-division, and/or frequency division processing.

Claim 17 (Newly Added): The base station transceiver of Claim 9, wherein the computation units are flexibly configured and connected to perform any one of several different transceiver functions.

Claim 18 (Newly Added): The base station transceiver of Claim 9, wherein the computation units are configured to perform one or more of downconversion, dechannelization, demodulation, decoding, equalization, despreading, encoding, modulation, spreading, and diversity processing.

Claim 19 (Newly Added): The base station transceiver of Claim 9, wherein the computation units support time-division, code-division, and/or frequency division processing.

Claim 20 (Newly Added): The method of Claim 10, wherein the computation units are flexibly configured and connected to perform any one of several different functions of the base station transceiver.

Claim 21 (Newly Added): The method of Claim 10, wherein the computation units are configured to perform one or more of downconversion, dechannelization, demodulation, decoding, equalization, despreading, encoding, modulation, spreading, and diversity processing.

Claim 22 (Newly Added): The method of Claim 10, wherein the computation units support time-division, code-division, and/or frequency division processing.